What is Claimed is:

1. A semiconductor device comprising a source region, a channel region, a drain region, a gate electrode formed on the channel region, and a drift region formed between the channel region and the drain region,

wherein the drift region is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region.

2. A semiconductor device comprising:

a first conductivity type well region formed in a first conductivity type semiconductor substrate;

a gate electrode formed on the substrate via a gate insulating film;

a first conductivity type body region formed to be adjacent to the gate electrode;

a second conductivity type source region and a channel region formed in the first conductivity type body region;

a second conductivity type drain region formed at a position remote from the first conductivity type body region; and

a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below the gate electrode, and formed deeply in a neighborhood of the drain region.

3. A semiconductor device according to claim 2, wherein the second conductivity type drift region is formed by implanting at least two kind second conductivity type impurities which have

different diffusion coefficients and at least one kind first conductivity type impurity which has a diffusion coefficient substantially equal to or larger than the diffusion coefficient of at least one kind second conductivity type impurity such that it is formed by diffusing the second conductivity type impurities into a deep region by using a difference in the diffusion coefficients and is formed shallowly in a neighborhood of the source region by canceling the second conductivity type impurities by the first conductivity type impurity.

4. A semiconductor device according to claim 3, wherein the second conductivity type drift region is formed by implanting an arsenic ion and a phosphorus ion as the second conductivity type impurities into an overall surface of a region serving as the drift region and selectively implanting a boron ion as the first conductivity type impurity only into a region in a neighborhood of the source region.

5. A method of manufacturing a semiconductor device including a first conductivity type well region formed in a first conductivity type semiconductor substrate, a gate electrode formed on the substrate via a gate insulating film, a first conductivity type body region formed to be adjacent to the gate electrode, a second conductivity type source region and a channel region formed in the first conductivity type body region, a second conductivity type drain region formed at a position remote from the first conductivity type body region, and a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below

the gate electrode, and formed deeply in a neighborhood of the drain region,

wherein the steps of forming the drift region, comprising the steps of:

implanting two kind second conductivity type impurities to form a second conductivity type low concentration layer constituting the drift region in the first conductivity type well region in the first conductivity type semiconductor substrate via postprocessing;

implanting selectively the first conductivity type impurity into a region located in a neighborhood of the source region; and

diffusing impurities under a condition that a diffusion coefficient of the first conductivity type impurity is set equal to or larger than a larger one of diffusion coefficients of the second conductivity type impurities.

6. A method of manufacturing a semiconductor device, comprising the steps of:

ion-implanting two kind second conductivity type impurities to form a second conductivity type low concentration layer serving as a drift region in a first conductivity type well region in a first conductivity type semiconductor substrate via postprocessing;

forming a LOCOS oxide film by oxidizing selectively a certain region on the substrate, and forming the second conductivity type low concentration layer at a relatively deep position in the first conductivity type well region and on a surface layer of the substrate by using a difference in diffusion coefficients of two kind second conductivity type impurities respectively;

ion-implanting and diffusing a first conductivity type impurity into the surface layer of the substrate of a source forming region via a mask which is formed on a drain forming region on the substrate so as to cancel the second conductivity type layer formed at the relatively deep position in the first conductivity type well region of the source forming region by a diffusion of the first conductivity type impurity;

forming a gate insulating film on the substrate, then forming a gate electrode to extend from the gate insulating film to the LOCOS oxide film, and then forming a first conductivity type body region adjacently to one end portion of the gate electrode by implanting and diffusing the first conductivity type impurity via a mask which is formed to cover the gate electrode and the drain forming region; and

forming a source/drain region by implanting the second conductivity type impurities via a mask having opening portions which are located over the source forming region and the drain forming region being formed in the first conductivity type body region.

7. A method of manufacturing a semiconductor device, according to claim 6, wherein the second conductivity type low concentration layer serving as the drift region is formed by implanting two kind second conductivity type impurities which have different diffusion coefficients and the first conductivity type impurity which has a diffusion coefficient substantially equal to or larger than the diffusion coefficient of one kind second conductivity type impurity of two kind second conductivity type

impurities such that it is formed by diffusing the second conductivity type impurities into a deep region by using a difference in the diffusion coefficients and also formed shallowly in a neighborhood of the source region by canceling the second conductivity type impurities by the first conductivity type impurity.

8. A semiconductor device comprising a first MOS transistor having a source region, a channel region, a drain region, a gate electrode formed on the channel region, and a drift region formed between the channel region and the drain region, and a second MOS transistor having a source region, a channel region, a drain region, and a gate electrode formed on the channel region,

wherein the drift region of the first MOS transistor is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region and

a source/drain region of the second MOS transistor consists of a low concentration source-drain region, a high concentration source-drain region, and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region.

9. A semiconductor device comprising a first MOS transistor and a second MOS transistor formed on a first conductivity type semiconductor substrate;

wherein the first MOS transistor includes,

a first conductivity type well region formed in the

semiconductor substrate,

a first gate electrode formed on the first conductivity type well region via a first gate insulating film,

a first conductivity type body region formed to be adjacent to the first gate electrode,

a second conductivity type source region and a channel region formed in the first conductivity type body region,

a second conductivity type drain region formed at a position remote from the first conductivity type body region, and

a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below the gate electrode, and formed deeply in a neighborhood of the drain region, and

wherein the second MOS transistor includes,

a second conductivity type well region formed in the semiconductor substrate,

a second gate electrode formed on the second conductivity type well region via a second gate insulating film, and

a source/drain region consisting of a low concentration source/drain region formed to be adjacent to the second gate electrode, a high concentration source/drain region, and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region.

10. A semiconductor device according to claim 9, wherein the first MOS transistor consists of an N-channel LDMOS transistor, and

the second MOS transistor consists of a P-channel high breakdown voltage MOS transistor.

11. A method of manufacturing a semiconductor device which includes a first MOS transistor having a body region in which a source region and a channel region are formed, a drain region separated from the body region, a gate electrode formed on the channel region, and a drift region formed between the channel region and the drain region, and a second MOS transistor having a source region, a channel region, a drain region, and a gate electrode formed on the channel region,

steps of forming a source/drain region of the second MOS transistor comprising at least a same step as the step of forming the body region of the first MOS transistor.

12. A method of manufacturing a semiconductor device, according to claim 11, wherein the step of forming the source/drain region of the second MOS transistor has at least a same step as the step of forming the drift region.

13. A method of manufacturing a semiconductor device according to claim 11,in which a first MOS transistor and a second MOS transistor are formed on a first conductivity type semiconductor substrate, comprising the steps of:

ion-implanting two kind second conductivity type impurities having a different diffusion coefficient via a mask which has an opening portion over a part of a first conductivity type well region on a first conductivity type semiconductor substrate on which the

first conductivity type well region and a second conductivity type well region are formed;

forming an oxidation resisting film in a certain region on the substrate, then forming a LOCOS oxide film by oxidizing selectively the substrate while using the oxidation resisting film as a mask, and forming second conductivity type low concentration layers at a relatively deep position in the first conductivity type well region and on a surface layer of the substrate by using a difference in diffusion coefficients of two kind second conductivity type impurities respectively;

ion-implanting and diffusing a first conductivity type impurity into a source forming region in the first conductivity type well region and the surface layer of the substrate in a source/drain forming region in the second conductivity type well region via a mask, which has opening portions over the source forming region in the first conductivity type well region and the source/drain forming region in the second conductivity type well region, so as to cancel the second conductivity type layer formed at the relatively deep position in the source forming region in the first conductivity type well region by a diffusion of the first conductivity type impurity and to form a first conductivity type source/drain region in the source/drain forming region in the second conductivity type well region;

forming a first gate insulating film in a region other than the LOCOS oxide film on the first conductivity type well region, and forming a second gate insulating film in a region other than the LOCOS oxide film on the second conductivity type well region;

forming a first gate electrode and a second gate electrode

on the first gate insulating film and the second gate insulating film respectively;

ion-implanting and diffusing the first conductivity type impurity via a mask, which covers the first gate electrode in the first conductivity type well region and the drain forming region and has an opening portion over a part of the source/drain forming region on the second conductivity type well region, so as to form a first conductivity type body region adjacently to one end portion of the first gate electrode and to form a second first conductivity type source/drain region in a region separated from the second gate electrode;

forming a first second conductivity type source region by implanting the second conductivity type impurities via a mask having an opening portion located over the source forming region in the first conductivity type well region;

forming sidewall spacer films on side wall portions of the first gate electrode and the second gate electrode, and then forming a second first conductivity type source/drain region by implanting the first conductivity type impurity via a mask having an opening portion located over the source/drain forming region in the first conductivity type well region; and

forming a third first conductivity type source/drain region by implanting the first conductivity type impurity via a mask having at least an opening portion, which is smaller than the second first conductivity type source/drain region, located over the second conductivity type well region.

14. A method of manufacturing a semiconductor device

according to claim 13, wherein the second conductivity type low concentration layer is formed by utilizing a difference in diffusion coefficients between two type second conductivity type impurities having a different diffusion coefficient and the first conductivity impurity having a diffusion coefficient which is almost equal to or larger than a diffusion coefficient of one of the second conductivity type impurities.

15. A method of manufacturing a semiconductor device according to claim 13, wherein concentration of the second first conductivity type source/drain region is set to a middle concentration which is higher than a concentration of the first conductivity type source/drain region but lower than a concentration of the third first conductivity type source/drain region.

16. A method of manufacturing a semiconductor device according to claim 11, wherein the first MOS transistor consists of an N-channel LDMOS transistor, and the second MOS transistor consists of a P-channel high breakdown voltage MOS transistor.

17. A semiconductor device according to claim 1, wherein the semiconductor device is arranged in plural via a element isolation film, and

a channel stopper layer is formed under the element isolation film.

18. A method of manufacturing a semiconductor device

according to claim 6, further comprising the steps of:

ion-implanting two kind second conductivity type impurities to form the second conductivity type low concentration layer serving as the drift region in the first conductivity type well region in the first conductivity type semiconductor substrate via postprocessing;

forming an oxidation resisting film on the substrate, and then ion-implanting the first conductivity type impurity into a surface of the substrate via a mask which is formed to cover the oxidation resisting film;

forming a first LOCOS oxide film and a second LOCOS oxide film by oxidizing selectively certain regions on the substrate while using the oxidation resisting film as a mask, and forming the second conductivity type low concentration layer at a relatively deep position in the first conductivity type well region and on a surface layer of the substrate respectively by using a difference in diffusion coefficients of two kind second conductivity type impurities, and then forming a channel stopper layer under the second LOCOS oxide film;

ion-implanting and diffusing the first conductivity type impurity into the surface layer of the substrate in the source forming region via a mask which is formed in the drain forming region on the substrate so as to cancel the second conductivity type layer formed at the relatively deep position in the first conductivity type well region in the source forming region by the diffusion of the first conductivity type impurity;

forming the gate insulating film in a region other than the first LOCOS oxide film and the second LOCOS oxide film on the

substrate, then forming the gate electrode to extend from the gate insulating film to the first LOCOS oxide film, and then forming the first conductivity type body region adjacently to one end portion of the gate electrode by implanting and diffusing the first conductivity type impurity via a mask which is formed to cover the gate electrode and the drain forming region; and

forming the source/drain region by implanting the second conductivity type impurities via a mask having opening portions which are located over the source forming region and the drain forming region formed in the first conductivity type body region.